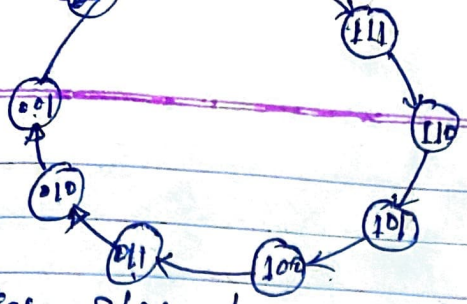


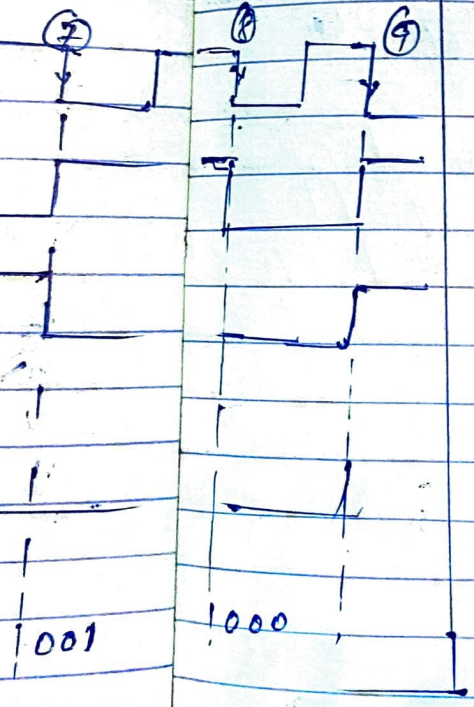
Fig: State diagram of a 3-bit ripple counter.

Drawbacks of Ripple counter:

1) Every flip-flop has its own propagation delay as output of previous FF is used as clock for the next FF.
2) Hence, the propagation delay goes on accumulating. For a 3-bit ripple counter the propagation delay of first FF gets added to that of second FF to decide the transmission time of the third stage.
3) So, with increasing no. of flip-flop propagation time increases.
4) So, There will be limitation on the maximum clock frequency.
5) The frequency f of a clock pulse for reliable counting operation is given by

$$f \leq \frac{1}{n(t_d) + T_s}$$

where
n = No. of flip flops
T_s = width of strobe pulse
t_d = propagation delay of one flip flop.



UP/DOWN COUNTERS

Up/down counter: An up/down counter is a combination of an up counter and a down counter. It can count in both direction

Types of Up/Down counters:
i) Up/down ripple counter (Asynchronous counter).
ii) Up/Down synchronous counter.

i) Up/DOWN Ripple counter: In the up/down ripple counter all the FFs are operated in the toggle mode. Hence, either T flip-flop or J-K flops are to be used. The LSB flip-flop receives clock directly however the clock to every other FF is obtained from Q or $\bar{Q}$ output of the previous FF.

- Up counting Mode (M=0): In this mode, the Q output of preceding FF is connected to the clock of next stage FF. For this mode M is connected at logic 0.
- DOWN counting Mode (M=1): In this mode $\bar{Q}$ output of the preceding FF is connected to the clock of the next FF. For this we connect M=1.

UP/DOWN 4-BIT ASYNCRONOUS COUNTER.

The below circuit diagram show the circuit diagram of a 4-bit up/down counter.

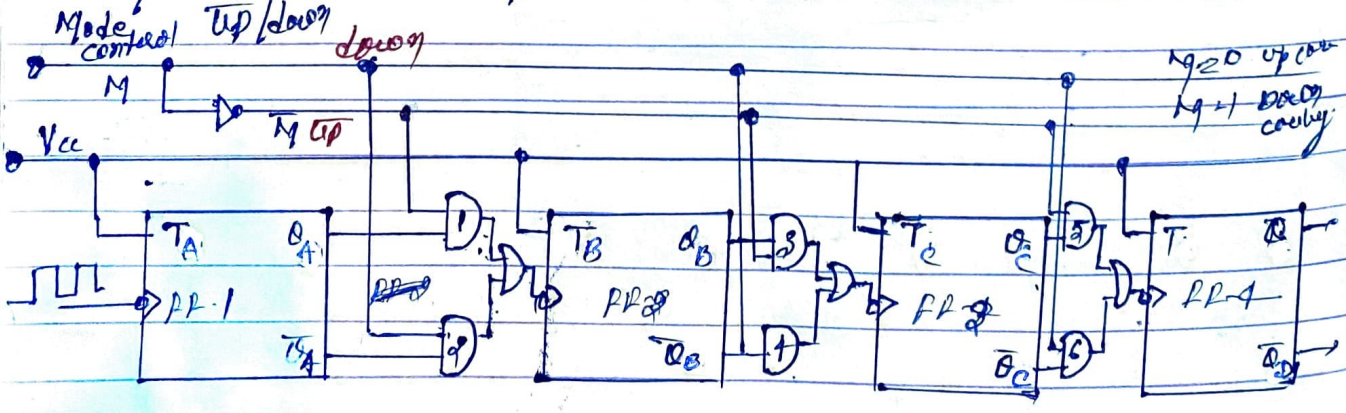


Fig: 4-bit up/down ripple counter.

operation Let $Q_D Q_C Q_B Q_A = 0000$

1) With M=0 (up counting Mode): With M=0, Gates 1, 3, 5, are enabled, whereas 2, 4, 6 are disabled. So, with the first falling edge of clock signal FF-1 is activated and remaining are off due to +ve applied signal to clock inputs of every clock signal. Hence, output state is $Q_D Q_C Q_B Q_A = 0001$

Now, with 2nd falling edge of clock signal FF-2 activated and remaining are off so, state will be $Q_D Q_C Q_B Q_A = 0010$.

So, the state are change continuously with the -ve falling edge of clock signal. to 1111 $2_D Q_C Q_B$

II) With M=1 (Down counting mode):- Under this case AND gates 2, 4 and 6 are enabled; whereas 1, 3, 5 gates are disabled and capable work as down counter.

With the 1st falling edge of clock signal, output of gate-2, 4, and 6 are 0 and also of 1, 3, 5 so CLK input of the all FF are activated and hence outputs of FFs are 1s. i.e $Q_D Q_C Q_B Q_A = 1111$.

On 2nd falling edge of clock signal, $Q_A = 0$, $Q_B = 1$, $Q_C = 1$, $Q_D = 1$ i.e $Q_D Q_C Q_B Q_A = 1110$

On 3rd falling edge of clock signal, $Q_D Q_C Q_B A = 1101$ and so on changes.

MODULUS OF THE COUNTER. (MOD-n COUNTER)

Modulus of a counter:- Modulus of a counter is defined as the number of states through which the counter progresses during its operation.

So, mod no. of the counter is given by the following expression,

Mod number = 2^n where n = No. of FFs.